Particle-Induced Mitigation of SEU Sensitivity in High Data Rate GaAs HIGFET Technologies

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Abstract

Proton and heavy ion data on two GaAs HIGFET logic families, one source coupled (SCFL) and the other complementary (C-HIGFET), show the importance of dynamic testing and develop a new technique for mitigating SEU sensitivity by minimizing charge enhancement effects.

I. Introduction

The complementary heterostructure insulated gate FET (C-HIGFET) and the source coupled FET logic (SCFL) cell families fabricated in GaAs are promising low-power alternatives to conventional high speed solutions such as GaAs E/D MESFET and Si ECL. C-HIGFET offers the power characteristics of a complementary cell type, and the high speed and total ionizing dose immunity of GaAs [1,2]. Though power consumption is somewhat greater than for C-HIGFET, the n-channel SCFL HIGFET family extends the speed capabilities well beyond the ~300 megabit per second (Mbps) limit of the complementary cell family. Together these families will benefit emerging satellite applications for processing digital data at rates up to several Gbps. Conventional alternative high speed technologies such as GaAs MESFET or silicon ECL impose severe power penalties along with unacceptable SEU rates for many satellite applications [3].

Hughlock et al. reported the first indication of heavy ion SEU characteristics for the C-HIGFET technology with studies on a 4-bit latch [4]. We extended these results with SEU tests of a C-HIGFET 1K SRAM covering protons and a range of linear energy transfer (LET) values using heavy ions obtained at the Brookhaven National Laboratory (BNL) Tandem Van de Graaff [5]. In this study we present test results and analysis to evaluate the SEU and displacement damage characteristics of C-HIGFET and SCFL shift registers operating at speeds of 200 and 400 Mbps. We compare these findings with static SEU measurements on these same devices, and with previously reported proton and heavy ions SEU studies [5]. This comparison highlights the need for dynamic testing of devices for which the intended application is at high speed in orbital particle environments. This builds on several other studies which have demonstrated the importance of testing at speed [6,7,8].

Following this comparison, we present data to support the claim that significant reductions in the SEU cross-sections for these devices can result from high fluence particle bombardment. We then explore a semiquantitative treatment of this behavior based on the relation between the amount of nonionizing energy deposited (displacement damage) and the resulting reduction in the carrier lifetime in the substrate. This lifetime affects charge enhancement dynamics (backgating and parasitic bipolar mechanisms) which are believed to dominate upsets in GaAs FET devices [9,10].

II. C-HIGFET and SCFL Test Structures

To extend previous static SEU studies to clocked logic and further examine the GaAs C-HIGFET and SCFL families, we have acquired a complete data set including total ionizing dose, displacement damage, and both heavy ion and proton upset cross-section measurements on two 32 bit serial shift registers fabricated by Motorola in a 1.0 μm process. This process has evolved from the HIGFET process licensed to Motorola by Honeywell, and the FET structures are essentially the same as those used in the fabrication of the 1K SRAM studied in [5].

The C-HIGFET devices examined in this work are based on a delta-doped complementary heterostructure insulated gate field effect transistor technology

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developed by Honeywell [2]. Conduction is provided in the n-device by a two dimensional electron gas formed at the AlGaAs - InGaAs interface. The channel is created in a quantum well due to a discontinuity in the conduction energy band at the undoped AlGaAs - InGaAs interface. Very high carrier mobilities are achieved in the two dimensional gas due to the lack of impurity scattering. It is also similar to CMOS technology in that the AlGaAs layer in the device isolates the gate from the channel for biases below V_{gs} = 1.3 V. The C-HIGFET technology provides a voltage swing 2-3 times larger than GaAs E/D MESFET. SPICE simulations indicating a critical charge of about 50 fC were reported in [5].

The 32 bit C-HIGFET shift register studied here can be operated at data rates approaching 300 Mbps. The SCFL 32 bit shift register supported data rates approaching 1 Gbps in an optimized test setup, but remote operation for particle beam studies limited our test conditions to operation at $\leq$ 400 Mbps. It is important to note that the two shift register types were fabricated using the same process with identical structures on the same die and differ only in the circuit bandwidth and the presence of the implanted p-channel devices in the complementary design. Common power busses to the chip supplied both C-HIGFET and SCFL circuitry, and total chip power did not exceed 500 mW at 400 Mbps. We believe most of this supported the source coupled FET logic.

III. Test Data and Analysis

Here we report new proton and heavy ion test data on shift register upset cross-sections obtained during static operation and while clocked at high data rates. Proton tests were conducted at the NRL beamline at the U.C. Davis Crocker Nuclear Laboratory using protons with

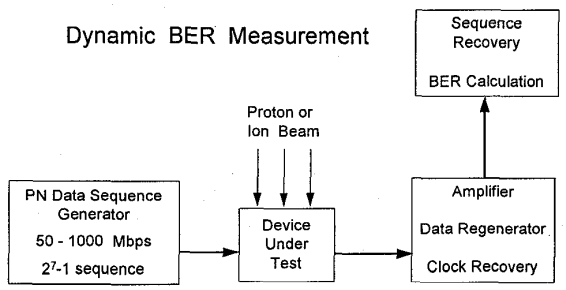

Figure 1. Pseudorandom data is clocked through the shift register DUT at high data rates during exposure.

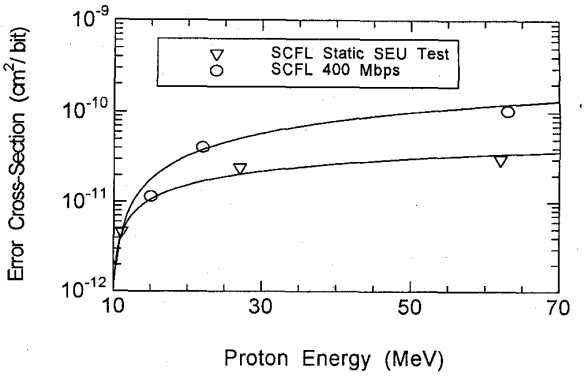

Figure 2. Shift register upset cross-section proton energy dependence for static vs. 400 Mbps operation.

energies ranging from 12 to 63 MeV, and heavy ion tests were carried out at BNL with the following ions: 98 MeV C-12, 138 MeV F-19, 209 MeV Cl-35, 280 MeV Ni-58 and320 MeV I-127. These ions enable us to clearly delineate, with good statistics, the cross section versus LET relations.

In addition to the traditional SEU characterization, we considered the effects of high particle fluences as they cause displacement damage and the formation of carrier recombination sites. The expectation was that the charge enhancement process would be minimized by the decreased carrier lifetime in the substrate. For these purposes, we tracked the damage induced by each of the particle types previously mentioned and also provided high fluence incremental exposures of 15 MeV protons and 320 MeV I-127 ions.

One important (and we believe general) result of this investigation involves the dependence of the bit-error cross-section on the data rate. We have made comparisons of static upset testing of the shift registers in which the pattern is clocked in prior to exposure and then interrogated for flipped bits post-exposure versus dynamic testing for which there is continual clocking of data at rates of 200 and 400 Mbps during exposure. The dynamic tests were conducted with a commercially available bit error rate test set [11] using a (2^7-1) pseudorandom data sequence as shown in figure 1.

A. Static versus Dynamic Test Results

Figures 2 and 3 illustrate the comparison of static versus dynamic operation for proton-induced and heavy ion-induced upsets respectively, and these figures also reveal the SEU response of the C-HIGFET and SCFL technologies. In all cases, we express the SEE

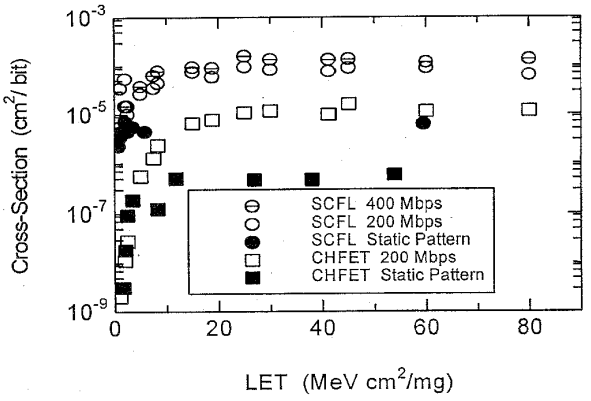

Figure 3. C-HIGFET and SCFL heavy ion upset cross-sections comparing static and 200 or 400 Mbps rates.

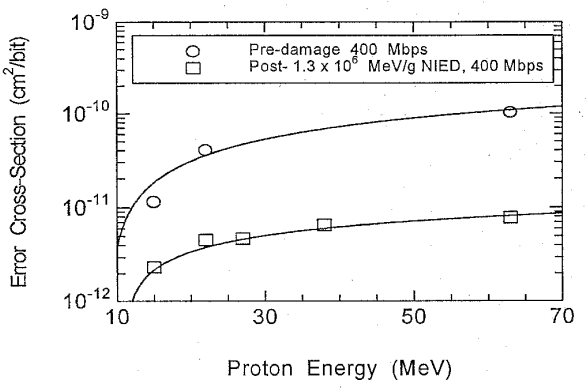

Figure 4. Proton cross-sections in the SCFL device are greatly reduced by particle-induced damage which surpresses backgating.

sensitivity in terms of a bit error cross-section per spatial bit and express it, as is customary, in units of area. We calculate this as the number of measured errors divided by the particle fluence and the number of serial stages in the shift register, which in this case is 32. Figure 2, showing proton bit error cross-section versus energy, indicates a sensitivity to even low energy (<15 MeV) protons in the SCFL family, though the C-HIGFET shift register could only be upset with proton energies above 40 MeV, and then with insufficient statistics to determine a reliable measure of the cross-section (σ), though it appears to be $< 10^{-13}$ cm^2/bit. This is consistent with results in [5] which indicated a relatively small proton upset cross-section of $< 10^{-13}$ cm^2 for static SRAM tests. The data of the figure do suggest significant increases in σ for the 400 Mbps clocked pattern which appears to exceed the static σ by a factor of 3.

Figure 3 data also reveal the greater sensitivity of the SCFL family relative to C-HIGFET logic for the case of heavy ions. The saturated cross-sections differ by nearly an order-of-magnitude between the complementary and source coupled circuits when tested under the same conditions, though both could be upset with LET values in the vicinity of 1 MeV$*$cm^2/mg. Again, these data are consistent with previous studies where comparison is possible. Specifically, under static test conditions the heavy ion LET threshold of about 1 MeV$*$cm^2/mg, and the saturated cross-section value of just under 10^{-6} cm^2 for the C-HIGFET SRAM reported in [5] are in close agreement with the static measurements for the corresponding shift register reported here in figure 3.

Further examination of figure 3 reveals the importance of testing the device at speed, especially if that reflects the intended flight application. For both the SCFL and C-HIGFET shift registers, the dynamic tests indicate cross-sections exceeding the static values by over an order-of-magnitude. And, for the SCFL device, the 400 Mbps cross-sections are consistently larger than the 200 Mbps values.

We offer two possible qualitative explanations for the increased sensitivity of the device during high speed operation. Recognizing that the static test condition offers an evaluation of the susceptibility of spatially separated sensitive nodes under unchanging conditions, during high speed operation there are likely other sensitive circuit elements or targets in addition to those upsettable during static conditions (e.g. clock distribution). Also, during fast operation, a given circuit element may spend a large fraction time in a state of increased sensitivity where noise margins are less than under static conditions. In [8] it was shown, by using pulsed laser testing, that the circuit examined in that study was most sensitive when the fast laser pulse arrived near the clock edge. Our future plans call for pulsed laser SEU testing of similar shift registers to examine both the temporal dependence of circuit elements which exhibit sensitivity during static conditions, as well as the possible increased susceptibility of targets which can not be easily upset under static conditions.

With these arguments in mind, it is interesting to note the relationship between the 200 and 400 Mbps data sets. We see an approximate cross-section

proportionality with data rate. To the extent that the measured cross-section reflects the amount of time the circuit sensitivity exhibits an enhanced temporal dependence (e.g. clock edge related), we would expect the doubling of the number of clock edges to represent a doubling in the number of opportunities for upsets, and this would lead to the observed proportionality with data rate. Future studies are planned to discover the details of this dependence, which may hold over some range of data rates, but will likely break down near the maximum circuit operating frequencies where SEU sensitivity might be expected to increase dramatically.

B. Cross-section Reduction with Ion Fluence

Though the cross-sections shown in the previous section are significantly greater in comparison with SEU high speed alternative technologies such as ECL and other GaAs technologies. These large cross-sections can present a potential problem for many satellite applications. Here we examine the hypothesis that substantial reductions in the upset cross-section can be attained by reducing the carrier lifetime in the substrate, and thereby minimizing the importance of charge enhancement effects. One technique for accomplishing this is particle-induced displacement damage which offers the following advantages. First, for study purposes, it is convenient to deliver the damage at the same facility (and indeed with the same ion beams) used in the SEU characterization. Also, this involves a post-fabrication step, so it could possibly be invoked to improve performance with no impact on an existing process per-se, though the possibility certainly exists for damage introduction with a high energy implanter following the high temperature processing stages.

In Figure 4 we show a summary of the proton-induced changes in the SCFL shift-register. For 400 Mbps operation, the two curves of the figure compare the cross-section proton energy dependence prior to irradiation with that following the high fluence exposure. The 63 MeV cross-section was reduced by over an order-of-magnitude by the deposition of 8.3 x 10^{11} MeV/g(GaAs) of nonionizing energy. This was delivered by high proton fluences at various energies (mostly 15 MeV) with a cumulative fluence of 1.8 x 10^{14} p/cm^2 and a corresponding total ionizing dose of > 50 Mrad(GaAs).

Figure 5 further supports the assertion that damage reduces the cross-section by comparing the heavy ion cross-section dependencies on LET between the proton-exposed device of Figure 4 with that of a "virgin" device. The comparison is made on the SCFL shift register at both the 200 Mbps and 400 Mbps data rates. Inspection of the Figure suggests the order-of-magnitude improvement covers the range of LET values from 1 to 90 MeV$*$cm^2/mg. Further, the triangle symbol tracks the monotonic decrease in σ we observed with increasing ion exposure on the "virgin" device subjected to normally incident 320 MeV I-127 ions. This again indicates the efficacy of damage for mitigating SEU sensitivity while not affecting normal device operation. We further note that the device leakage currents actually decreased slightly over the course of the damage studies.

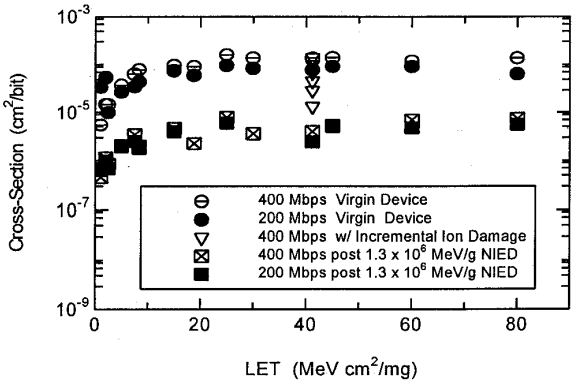

Figure 5. Heavy ion cross-sections for the SCFL parts are reduced >10x by particle-induced damage to mitigate backgating, without altering normal operation up to 400 Mbps.

Detailed quantitative evaluation of the carrier lifetime changes in the semi-insulating substrate and the resulting changes in the SEU susceptibility are beyond the scope of the present work. Even so, the data shown here, along with the qualitative understanding that carrier lifetime changes affect the enhanced charge collection mechanisms responsible for upsets, are consistent with the modeling results described in [9]. Also, we note that damage as a way of modifying the substrate carrier lifetime is not the only approach. In fact, recent investigations of the use of a low temperature grown GaAs epitaxial for control of substrate carrier lifetimes has shown that the problem of SEE in GaAs may be eliminated entirely [12-14]. Both the low temperature (LT)-GaAs approach and the particle-induced damage approach rely on the

suppression of parasitic bipolar and backgating charge mechanisms through the rapid recombination of charge deposited in the region beneath the channel.

For the case of particle-induced damage, figure 6 graphically illustrates the reduction in SEU cross-section following from incremental proton and heavy ion exposure. The damage energy is calculated using the nonionizing energy loss rate for protons and heavy ions, and expressed in MeV / g (GaAs).

Though it is not the focus of this present work, we do note that an alternate approach exists for circuit level hardening of the SCFL circuitry examined here. Motorola has recently demonstrated a circuit based SEU hardening technique which results in 3 to 4 order-of-magnitude reductions in the cross-sections reported here. Saturated cross-sections of approximately 10^{-9} cm^2 result. This technique applied to SCFL GaAs as well as CML/ECL silicon circuits, imposes minimal power and area penalties, and preserves the high bandwidth inherent in these logic families.

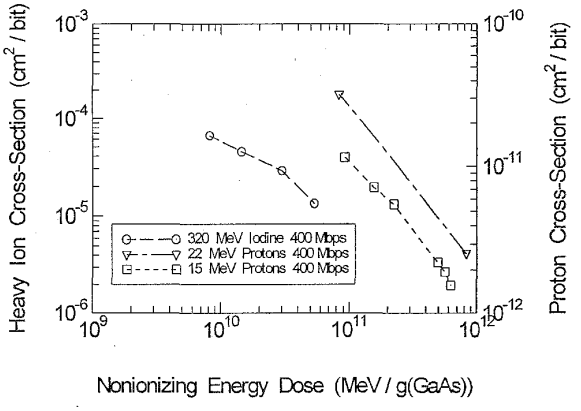

Figure 6. Proton and heavy ion upset cross-sections in the SCFL device at 400 Mbps are significantly reduced by accumulated nonionizing energy deposition.

IV. Conclusions

We have examined the SEU characteristics of two important new GaAs logic families and found their response to be better than other high speed logic families. Also, we have compared traditional "static" measurement techniques with results from dynamic tests up to 400 Mbps, and we show order-of-magnitude increases in the saturation cross-section at the higher speed, thus pointing to the importance of testing at the speed of intended operation. Finally, by modifying the dynamics of the backgating and parasitic bipolar charge enhancement effects, we have developed and validated an approach to mitigate the SEU sensitivity of these technologies. Initial results of substrate carrier lifetime reduction by nonionizing energy deposition indicate order-of-magnitude improvement with no apparent negative effect on normal device operation.

V. References

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